ETHERNET SYSTEM

This invention relates to systems for, and methods of, operating in local area networks to provide for the transmission and reception of signals through unshielded twisted 5 pairs of wires between a computer and a hub. The invention particularly relates to systems for, and methods of, using digital techniques for enhancing the recovery, and the quality of such recovery, of the digital signals passing through the unshielded twisted pairs to the computer so that the 10 information represented by such digital signals can be restored at the computer.

Systems now exist for passing information between different computers in a local area network. The systems include a hub connected to computers located at spaced 15 positions around the hub. The connections between the hub and each computer are generally through unshielded twisted pairs of wires. These wires are generally made from copper so that they have relatively large losses. This has limited the distance through which the signals can pass between the hub 20 and each computer. The unshielded twisted pairs of wires have also limited the rate at which the signals can be transmitted. Until relatively recently, the distance between the hub and each computer has been limited to approximately one hundred (100 m.) and the rate of signal trans- 25 mission has been limited to approximately 10 megabits per second (10 Mb/sec.).

The systems discussed in the previous paragraph and constituting the prior art have used analog techniques at the computer to recover the information represented by the 30 digital signals. For example, the systems of the prior art have used analog equalizers to compensate for deteriorations in the characteristics of the digital signals as the digital signals pass through the unshielded twisted pairs of wires. These analog techniques have been satisfactory when the signals 35 have passed through the unshielded twisted pairs of wires at a frequency of ten megabits per second (10 Mb/sec.)

The amount of information being transmitted through the unshielded twisted pairs of lines has been increasing at a relatively rapid rate. To provide for this increased transmis- 40 sion of information, the rate of transmission has been increased to one hundred megabits per second (100 Mb/sec.). The increased rate of signal transmission has prevented analog equalizers from operating effectively in restoring at the computer the signals transmitted from the 45 hub.

Digital circuits have been considered for use in systems employing unshielded twisted pairs of wires and transmitting signals at one hundred megabits per second (100 Mb/sec) through distances as great as one hundred meters 50 (100 m.). For example, digital adaptive equalization technology has been considered for such systems. However, such digital systems have been rejected for several reasons. One reason has been that the systems considered have not provided significantly enhanced performance. Furthermore, 55 the complexity of such systems has been quite high, particularly in relation to any enhanced performance obtained from such systems. The cost of such digital systems has also been considered to be excessive.

This invention provides a system for, and method of, 60 receiving at a computer packets of digital signals transmitted from a hub displaced by a distance of as much as one hundred meters (100 m.) from the computer and for recovering the information represented by the digital signals in the packets. The system and method of this invention provide 65 for such recovery whether the digital signals are transmitted through the wires at a frequency of ten megabits per second

(10 Mb/sec.) or one hundred megabits per second (100 Mb/sec).

The system of this invention includes a digital adaptive equalizer for recovering the information represented by the digital signals in the packets. This equalizer is of an advanced design and includes feedback techniques to enhance the resolution provided by the equalizer in determining the amplitude level of each of the digital signals in each packet. The system and method of this invention are particularly adapted to operate with four (4) unshielded twisted pairs of wires, three (3) of the four (4) transmitting information whether the transmission is from the hub to the computer or from the computer to the hub. The system and method of this invention also include circuits and techniques for synchronizing the operation of the equalizer with the digital signals in the packets to enhance the recovery of the amplitudes of the digital signals by the equalizer.

In one embodiment of the invention, four (4) unshielded twisted pairs of wires connect a hub and a computer in an Ethernet system: one (1) pair of transmission only, another for reception only and the other two (2) both for transmission and reception. The signals in the wires are in packets each initially having timing signals defining a preamble and thereafter having digital signals representing information as by individual ones of three (3) amplitude levels.

The signals received at the computer are provided with an automatic gain control (AGC) and then with digital conversion at a particular rate. A control loop operative upon the digital conversions regulates the AGC gain at a particular value. An equalizer operative only during the occurrence of the digital signals representing information in each packet selects an individual one of the three (3) amplitude levels closest to the amplitude of each digital conversion at the time assumed to constitute the conversion peak.

The amplitudes of the timing signals in each preamble at the times assumed to constitute the peaks and zero crossings of such signals are multiplied. The rate of such digital conversions is adjusted in accordance with the polarity and magnitude of the multiplication product. The relative amplitudes of the successive equalizer values following each preamble are evaluated at the times assumed to be the peaks of the digital conversions. The rate of the digital conversions is adjusted in accordance with such evaluations, thereby further regulating the digital conversions at the particular rate. The equalizer thus operates on the information signals in each packet at the signal peaks.

In the drawings:

FIG. 1 is a schematic block diagram of an Ethernet system providing a plurality of computers connected to a hub by unshielded twisted pairs of wires to form a local area network (LAN);

FIG. 2 is a circuit diagram in block form of an overview of the hub and one of the computers in FIG. 1, the circuit diagram showing such computer and such hub, and connections of the unshielded twisted pairs of wires between them, when the computer receives packets of signals from the hub or transmits packet of signals to the hub;

FIG. 3 is a circuit diagram showing in block form the construction of the computer, and the unshielded twisted pairs of wires connected to the computer, when the computer operates to send packets of signals through the unshielded twisted pairs of wires to the hub;

FIG. 4 is a circuit diagram showing in block form the construction of the computer, and the connections of the unshielded twisted pairs of wires to the computer, when the computer operates to receive and decode packets of signals passing through the unshielded twisted pairs of wires from the hub;

3

provided between the hub 12 and the computer 14. The system shown in FIG. 1 is operative with several categories of twisted pairs of cables designated as categories 3, 4 and 5 in the telecommunications industry. Category 3 cables are

5 the poorest quality (and lowest cost) and category 5 cables are the best quality (and highest cost).

FIG. 2 provides an overview on a simplified basis of a system, generally indicated at 24, in which the features of this invention are incorporated. The system 24 as shown in

10 FIG. 2 is known in the prior art. The system 24 provides for a transmission of digital signals between one of the computers (e.g. the computer 14) and the hub 12 and the reception of such signals at the other of the computer and the hub. A similar system can be provided for each of the

15 computers 16, 18 and 20. The system includes four (4) unshielded twisted pairs (UTP) 22, 26, 28 and 30 of wires or cables. These unshielded twisted pairs of cable of respectively designated as Pair 1, Pair 2, Pair 3 and Pair 4 in FIG. 1.

20 An amplifier 32 at the computer 14 and an amplifier 34 at the hub 12 are connected to transmit digital signals through the unshielded twisted pairs 22 of wires only in the direction from the computer 14 to the hub 12. An amplifier 36 at the hub 12 and an amplifier 38 at the computer 14 are

25 connected to transmit digital signals through the unshielded twisted pair 26 of wires only from the hub 12 to the computer 14.

Each of the unshielded twisted pairs 28 and 30 of wires or cables is connected to pass signals from the hub 12 to the

30 computer 14 and also from the computer to the hub. This results from the connections of amplifiers 40 and 42 in opposite directions in the computer 14 to the unshielded twisted pairs 28 of wires or cables and from the connections of amplifiers 44 and 46 in opposite directions in the hub 12

35 to such unshielded twisted pairs of wires. Similar connections are made to the unshielded twisted pairs 30 of wires.

FIG. 3 provides an overview of the computer 14 when the computer operates as a transmitter. This overview is known in the art. It will be appreciated that similar over-

40 views may be provided for each of the computers 16, 18 and 20 when these computers operate as transmitters. As shown in FIG. 3, the computer 14 includes a media access controller 50. The controller 50 becomes operative when the computer 14 is simultaneously attempting to transmit and

45 receive packets of signals. At such a time, the controller 50 provides a selective priority to the signals being received or to the signals being transmitted. Preferably the priority may be to the packets of signals being received since these packets of signals may otherwise be lost.

50 The signals to be transmitted are introduced to an encoder 52 which encodes each of the signals to one (1) of three (3) amplitude levels dependent upon the information represented by such signal. The encoding of the signals to the individual ones of the three (3) amplitude levels effec-

55 tively provides a reduction in the frequency of the signals. The signals then pass to a data splitter 53 which operates as a demultiplexer to pass the signals in successive packets into successive ones of three (3) channels on a cyclic basis. This causes the frequency of the signals in the packets in each of

60 the channels to be reduced to one third ($\frac{1}{3}$) of the frequency of the packets of signals from the encoder 52.

One of the three (3) channels in FIG. 3 includes stages 54 for shaping the waves of the transmitted signals and also includes a filter/coupler 56 for limiting the frequency of the

65 signals and for coupling the filtered signals to an unshielded twisted pair (UTP) 58 (designated as Pair 1) of wires. Each of the other two channels also includes wave shaping stages

and filter/couplers respectively corresponding to the stages 54 and 56 in FIG. 3. These stages respectively introduce signals to unshielded twisted pairs 60 (designated as Pair 3) and 62 (designated as Pair 4).

In addition to passing through the unshielded twisted pairs 60 and 62 of wires on cables, the signals received by the computer 14 pass through an unshielded twisted pair 64 (designated as Pair 2), a filter/coupler 66 and a carrier sensor 68 to the media access controller 50 to activate the media access controller when a collision in the computer 14 between transmitted and received signals is about to occur.

FIG. 4 provides an overview of the computer 14 when the computer operates as a receiver. This overview is known in the art. It will be appreciated that similar overviews may be provided for each of the computers 16, 18 and 20 when these computers operate as receivers. As shown in FIG. 4, the packets of signals are received on the unshielded twisted pairs 64 (Pair 2), 60 (Pair 3) and 62 (Pair 4) of wires. The packets of signals on the unshielded twisted pair 64 of wires are introduced to the filter/coupler 66 and then to the data recovery stage 68 which recovers the individual one of the three amplitude levels provided for each signal in each packet. The stages 64, 66 and 68 are also shown in FIG. 3. A filter/coupler and a data recovery stage are also provided for each of the channels respectively associated with the unshielded twisted pairs 60 and 62 of wires.

The signals from the data recovery stage 68 and the other two (2) data recovery stages are introduced to a data combiner 70 which acts as a multiplexer to recombine the signals in the three (3) received channels. A decoder 72 then recovers the information represented by the individual ones of the three (3) amplitude levels for the successive signals in the packets. The decoded signals then pass to the media access controller 50 also shown in FIG. 3.

As previously described, the signals in the unshielded twisted pairs 58, 60, 62 and 64 of wires or cables have a data rate of one hundred megabits per second (100 Mb/sec.). The rate of the transmission of such signals is at twenty five megabauds per second (25 Mbaud/sec.). The signals are in packets each having signals identifying the beginning of such packet and each having, after such identifying signals, a plurality of timing signals at the beginning of such packet.

The timing signals are provided in preambles in the packets. There may illustratively be eighteen (18) timing signals in each packet. Each of the timing signals has two (2) amplitude levels (positive and negative). The timing signals for the different packets are respectively illustrated at 76a, 76b and 76c in FIG. 5 for the channels 64 (Pair 2), 60 (Pair 3) and 62 (Pair 4). The timing signals are provided in preambles in the packets. The timing signals in each packet are followed by digital signals representing information or data. The digital signals in each packet have individual ones of three (3) amplitude levels to represent the information or data.

Although the digital signals representing the data in the packets have a frequency of one hundred megabits (100 Mb/sec.) per second, this frequency is reduced by the encoder 52 as a result of the conversion of the signals to three (3) amplitude levels. The frequency of such digital signals is also reduced by the data splitter 53 in FIG. 3 as previously described. The resultant digital signals in each of the unshielded twisted pairs 60, 62 and 64 of wires has a frequency of thirty three megabits per second (33 Mb/sec.).

FIG. 6 provides a simplified block diagram of a system constituting one embodiment of this invention for transmitting such signals from a computer such as the computer 14 through the unshielded twisted pairs of wires (e.g. the pairs 58, 60 and 62) to the hub and for receiving such signals through the unshielded twisted pairs (e.g. 60, 62 and 64) of

wires at the computer from the hub and for processing such received signals at the computer to recover the information or data represented by such signals. The same block diagram (FIG. 6) also applies to each of the computers 16, 18 and 20.

5   The system shown in FIG. 6 includes the media access controller 50 (also shown in FIGS. 3 and 4), a stage 80 (which constitutes a combination of the encoder 52 and the data splitter 53 in FIG. 3) and transmitters 82a, 82b and 82c for passing the signals in the packets through the unshielded

10 twisted pairs 58 (Pair 1), 60 (Pair 3) and 62 (Pair 4) of wires or cables in FIG. 3. The signals received from the hub 12 pass through the unshielded twisted pairs 64 (Pair 2), 60 (Pair 3) and 62 (Pair 4) of wires or cables in FIG. 4. These signals are respectively received by receivers and equalizers

15 84a, 84b and 84c. The receivers and equalizers 84a, 84b and 84c are included within the features of this invention. They operate on a digital basis to select the individual ones of the three (3) amplitude levels closest to the amplitudes of the received digital signals.

20   The signals from the receivers and equalizers 84a, 84b and 84c pass to a clock recovery stage 86 which operates upon these signals to recover a clock signal. The stage 86 is included within the features of this invention. This clock signal is used to synchronize the operation of the receivers

25 and equalizers 84a, 84b and 84c and the data combiner and decoder 88. The clock signal from the stage 86 and the signals from the receivers and equalizers 84a, 84b and 84c are introduced to a stage 88 which constitutes a combination of the data combiner (or multiplexer) 70 and the decoder 72

30 in FIG. 4. The combination of the stages 84a, 84b, 84c, 86 and 88 is considered to be within the features of this invention. The signals from the stage 88 pass to the media access controller 50 also shown in FIGS. 3 and 4.

    FIG. 7 illustrates one of three receiving and equalizing

35 channels (see the receivers and equalizers 84a, 84b and 84c in FIG. 6) in the computer 14 in additional detail. It will be appreciated that each of the other two (2) receiving channels in the computer 14 may be constructed in the same or a similar manner. The same block diagram (FIG. 7) also

40 applies to the receiving and equalizing channels in the computers 16, 18 and 20. The receiver and equalizer shown in FIG. 7 are unique to this invention. The receiver and equalizer shown in FIG. 7 include an automatic gain control stage (AGC) 90 which is connected to receive the signals

45 passing through the unshielded twisted pair 64 of wires. The signals from the AGC stage 90 pass to an analog-to-digital (A-D) converter 92. The converter 92 provides digital conversions of the signals from the AGC stage 90 at a suitable frequency such as fifty megahertz (50 MHz), which is twice

50 the baud rate of the signals.

    The signals from the converter 92 pass to an AGC control loop 94. The signals from the AGC control loop 94 regulate the gain of the signals of the AGC stage 90 at a particular value. In this way, the amplitudes of the signals from the

55 converter 92 are independent of any variation in the gain in the signals. The rate of production of the digital conversions is regulated by a timing recovery stage generally indicated at 96 so that the digital conversions of the signals from the stage 92 are at a particular rate and in a particular phase. The

60 timing recovery stage 96 is shown in additional detail in subsequent Figures.

    The output from the converter 92 is introduced to a digital adaptive equalizer generally indicated at 98 in FIG. 7. The stages in the digital adaptive equalizer 98 are shown

65 within broken lines in FIG. 7. They include a feed forward equalizer 100 which is connected to the output of the A-D converter 92. A suitable feed forward equalizer for use as the

7

equalizer 100 is disclosed in an article entitled "A 100 MHz, 5M Baud Decision Feedback Equalizer for Digital Television Applications" written by Robindra B. Joshi and Henry Samueli and published in the IEEE International Solid-States Circuits Conference on Feb. 16, 1994. The output of the feed forward equalizer 100 is introduced to an adder 102 as is the output from a decision feedback equalizer 104. The output from the adder 102 passes to a three (3)-level data slicer 106. The output from the data slicer 106 constitutes the input to the decision feedback equalizer 104. The output from the data slicer 106 also provides the data or information represented by the three (3)-level digital signals following the timing signals in the preamble in each packet. The output from the data slicer 106 is provided on a line 109.

The adder 102 adds the outputs of the feed forward equalizer 100 and the decision feedback equalizer 104 to provide an output which is introduced to the slicer 106. This addition may be seen from FIG. 8. As will be seen in FIG. 8, a composite signal generally indicated at 108 is shown as being comprised respectively of left and right halves 108a and 108b. The feed forward equalizer 100 may be considered to correct for distortions in the left half 108a of the composite signal 108 and the decision feedback equalizer 104 may be considered to correct for distortions in the right half 108b of the composite signal 108. The distortions result in part from the fact that the digital signals representing information or data in each packet develop tails as they travel through the unshielded twisted pairs of wires. As a result of the corrections for these distortions, the adder 102 provides the value of the amplitude of the composite signal 108.

The output from the adder 102 is introduced to the slicer 106 in FIG. 7. The slicer 106 provides a plurality (e.g. 3) of progressive amplitude values and determines the particular one of the three (3) amplitude values closest to the output from the adder 102. The slicer 106 provides this value on the line 109 for each of the digital signals in each packet to indicate the data or information represented by such digital signals. In this way, the digital adaptive equalizer 98 restores the analog levels of the digital signals in the packets at the receiver to the analog levels of these digital signals at the hub 12 even with the distortions produced in these signals as they pass through the unshielded twisted pairs of wires.

FIG. 9 shows curves of different patterns of successive digital signals in the packets when the digital signals have individual ones of the three (3) amplitude levels and have a frequency of twenty five megahertz (25 MHz). In FIG. 9, time in 10^{-8} seconds is shown along the horizontal axis and relative amplitudes in positive and negative polarities are shown along the vertical axis. For example, three successive amplitude levels of +1, +1 and +1 are indicated at 110 in FIG. 9 and three successive amplitude levels of −1, −1 and −1 are indicated at 112 in that Figure. Similarly, three (3) successive amplitude levels of 0, +1 and 0 are indicated at 114 in FIG. 9 and three (3) successive amplitudes of +1, 0 and +1 are indicated at 116 in that Figure. Three successive amplitude levels of 0, 0, 0 are also indicated at 118 in FIG. 9 and three successive amplitudes of +1, −1 and +1 are also indicated at 120 in FIG. 1. FIG. 9 represents the desired (or perfect) wave forms for different combinations of three (3) successive digital signals in a packet.

FIGS. 10(a), 10(b) and 10(c) show the degradations in the signal combinations of FIG. 9 after the signals in such combinations have travelled different distances between the hub 12 and the computer 14. FIG. 10(a) shows the degradations in such signal combinations after the signals in such combinations have travelled a distance of approximately

8

thirty meters (30 m.) through one of the unshielded twisted pairs **64, 60** and **62** of wires.

FIG. 10(*b*) shows the further degradations in such signal combinations after the signals in such combinations have travelled a distance of approximately sixty meters (60 m.) through one of such unshielded twisted pairs of wires. The degradation in such signal combinations is further aggravated after the signals in such combinations have travelled a distance of approximately one hundred meters (100 m.) through one of the unshielded twisted pairs **64, 60** and **62** between the hub **12** and the computer **14**. This is shown in FIG. **10**(*c*).

This invention recovers in the computer **14** the pattern of the successive signals transmitted through each of the unshielded pairs **64, 60** and **62** of wires from the hub **12** even after such signals have travelled a distance of approximately one hundred meters (100 m.) from the hub and have suffered the degradation shown in FIG. **10**(*c*). As will be seen, clearing up the signal confusion shown in FIG. **10***c* to restore the signals shown in FIG. **9**, as by the system of this invention, constitutes a significant achievement.

FIG. **11** is a circuit diagram showing in additional detail the system shown in FIG. **7** with particular emphasis on the construction of the timing recovery block **96** in FIG. **7**. The system shown in FIG. **11** includes the A-D converter **92** and the equalizer **98** also shown in FIG. **7**. The A-D converter **92** receives on a line **122** clock signals at the master clock frequency of fifty megahertz (50 MHz). The A-D converter **92** provides outputs at the times assumed to be the peaks and zero crossings of the digital conversions from the converter **92**. The outputs from the A-D converter **92** are used in the system shown in FIG. **11** to adjust the phase of the master clock frequency so that the signals will actually be produced at the peaks and zero crossings of the master clock signals. The output at the time assumed to be the peak of the digital conversions is designated as "x_p" in FIG. **11** and the output at the time assumed to be the zero crossing is designated as "x_o" in FIG. **11**

The signal x_p from the converter **90** is shown in FIG. **11** as being introduced to the equalizer **98**. As previously described, the equalizer **98** operates upon the signal X_p to select the individual one of the three (3) amplitude levels closest in amplitude to the signal x_p. This amplitude level is designated in FIG. **11** as "$\hat{x}$". The signal $\hat{x}$ from the equalizer **98** is introduced to a low gain error generator **124** which is included within the timing recovery block **96** also shown in FIG. **7**. The stages included in the timing recovery block **96** are disposed within a rectangle shown in broken lines in FIG. **11**. This recovery block is generally indicated at **96** in FIGS. **7** and **11**. The low gain error generator **124** also receives the x_o output from the A-D converter **92** and provides an output, designated as a "low gain error", on a line **125** to a loop filter generally indicated at **126** and included within the timing recovery block **96**.

The loop filter **126** also receives clock signals on a line **128** at a baud clock rate of twenty five megahertz (25 MHz). The loop filter **126** additionally receives signals, designated as "boost & boost 2", on a line **130** from a high gain error generator **132**. Signals designated as "high gain error" are introduced on a line **134** from the high gain error generator **132** to the loop filter **126**. A phase inverter **136** provides signals (designated as "freeze") on a line **138** to the loop filter **126**. The output from the loop filter **126** passes through a line **140** to a ring voltage controlled oscillator (or ring oscillator) generally indicated at **186** in FIG. **16** and shown in additional detail in FIG. **16**.

9

The phase inverter **136** receives the clock signals on the line **122** at the master clock frequency of fifty megahertz (50 MHz) and clock signals at the baud clock frequency of twenty five megahertz (25 MHz). The clock signals on the line **128** also pass to internal blocks. The clock signals on the lines **122** and **128** also pass to a controller **142**. The controller **142** also receives on a line **144** signals which indicate the start of each packet. These signals are provided in a special pattern at the beginning of each packet. The controller **142** provides other control signals on a line **146**.

The signals x_p and x_o at the times respectively assumed to be the peaks and zero crossings of the timing signals **76a**, **76b** and **76c** (FIG. 5) pass from the A-D converter **92** to the high gain error generator **132**. FIG. 12 indicates the response of the high gain error generator **132** to the signals x_p and x_o generated during the occurrence of the timing signals in the preamble in each packet. The high gain error generator **132** multiplies the values of the signals x_p and x_o for each of the timing signals and determines from the multiplication product the correction, if any, which should be made in the times assumed for the peak x_p and the zero crossing x_o to occur.

When the product of x_p and x_o for a timing signal is zero, no correction has to be made since the time assumed by the baud clock signal on the line **128** to be the zero crossing for a timing signal is actually the time that the zero crossing has occurred. When the signal x_p occurs at a time indicated at **148** in FIG. 12(a) and the signal x_o occurs at a time indicated at **150** in FIG. 12(a), the product of x_p and x_o is positive. This indicates that the time assumed by the baud clock signal on the line **128** in FIG. 11 for the peak x_p and the zero crossing x_o to occur is early. As a result, the error generator **132** delays the phase of the baud clock signal on the line **128** in FIG. 11 so that the times assumed for the peak x_p and the zero crossing x_o to occur will approach the times that such peak x_p and such zero crossing x_o actually occur.

FIG. 13(b) provides another illustration of the times **152** and **154** respectively assumed for the peak x_p and the zero crossing x_o to occur in one of the timing cycles in the preamble of a packet. As will be seen, since x_o has a negative polarity and x_p has a positive polarity, the polarity of the product of x_p and x_o is negative. This indicates that x_p and x_o are occurring at a late time. The phases of the baud clock signals or the line **128** in FIG. 11 are accordingly shifted in a leading direction so that the times assumed for x_p and x_o to occur approach the time that x_p and x_o actually occur.

FIGS. 13(a) and 13(b) respectively show the same relationship in time between x_p and x_o as are shown in FIGS. 12(a) and 12(b). As will be seen in FIGS. 13(a) and 13(b) and also in FIGS. 12(a) and 12(b), a relatively small amount of a phase shift has to be made in the phase of the baud clock signals on the line **128** in FIG. 11 to bring the signal x_p in synchronism with the peak of the baud clock signals actually occurring on the line **128** and to bring the zero crossing x_o in synchronism with the zero crossing of the baud clock signals actually occurring on the line **128**. This may be seen from the fact that $|x_p|>K|x_o|$ in FIGS. 13(a) and 13(b) where K is a constant gain factor having a relatively high value greater than 1.

Sometimes, however, the baud clock signals on the line **128** are considerably out of synchronism with the signals x_p and x_o respectively assumed to constitute the peaks and zero crossings. This is shown in FIGS. 13(c) and 13(d). As will be seen in FIG. 13(c), the signals x_p and x_o are delayed relative to the baud clock signals on the line **128** by a phase angle less than, but approaching 90°. In FIG. 13(d), the signals x_p and x_o are delayed relative to the baud clock signals on the line **128** by a phase angle greater than 90°. In

both of these instances, $|x_p|<K|x_o|$. In both of these situations, synchronization between the baud clock signals on the line 128 on the one hand and the peak signal x_p and the zero crossing signal x_o on the other hand will occur on an
5 expedited basis when a phase shift (or phase inversion) of 90° is provided.

When the phase shift of 90° occurs in the time relationship shown in FIG. 13(c), the relative positions of the x_p and x_o signals in FIG. 13(c) will be shifted to the relative
10 positions of these signals in FIG. 13(a). Similarly, the relative positions of the x_p and x_o signals in FIG. 13(d) will be shifted to the relative positions of these signals in FIG. 13(b) when a phase shift of 90° is provided in these signals. Relatively minor corrections can thereafter be provided in the phase of the clock signals to have x_p correspond to the
15 peak of the baud clock signals on the line 128 and to have x_o correspond to the zero crossing of such baud clock signals.

The phase inverter 136 in FIG. 11 provides the phase shift of 90° discussed in the previous paragraph. The rela-
20 tionship shown in FIGS. 13(c) and 13(d) to create the phase inversion of 90° is advantageous because it minimizes false inversions resulting from large amplitudes of noise or from the trailing spikes that are produced as a result of the passage of the digital signals for a distance of one hundred meters
25 (100 m.) through the unshielded twisted pair of wires.

Only one phase shift of 90° is provided during the preamble in each packet. This is indicated by the "freeze" indication on the line 138 in FIG. 11. The reason for this is that more than one such phase shift in a preamble will tend
30 to create instability in the effort to synchronize the baud clock signal on the line 128 with the peak signal x_p and the zero crossing x_o during the occurrence of the timing signals in the preamble in each packet.

Furthermore, the phase shifts in the clock signals on the
35 line 128 in FIG. 11 are made only during a first limited number of timing signals in each preamble. This results from the introduction of a signal (designated as "time out") on a line 139 from the controller 142 to the phase inverter 136. For example, if there are eighteen (18) timing signals in each
40 preamble, the phase shifts in the clock signals on the line 128 will preferably be made only in the first ten (10) timing signals in such preamble. This prevents large amplitudes of noise in the last eight (8) timing signals of a preamble from producing undesired phase shifts of 90° in the clock baud
45 signals on the line 128. Such large phase shifts in the last timing signals in each preamble would tend to create instabilities, particularly when such large phase shifts result from the introduction of noise into the system.

Sometimes the gain of the signals from the converter 92
50 is relatively low. When the gain of the converter 92 as represented by the x_p and x_o signals is at least fifty percent (50%) below the dynamic range of the converter 92, a signal is introduced on the line 130 to the loop filter 126. This causes the loop gain to be doubled. The loop gain is doubled
55 again when the gain of the converter 92 as represented by the x_p and x_o signals is below twenty five percent (25%) of the dynamic range of the converter 92.

The low gain error generator 124 provides error corrections during the occurrence of the digital signals following
60 the timing signals in the preamble of each packet. These digital signals indicate the data or information in each packet. As a result of these error corrections, the phase of the digital conversions by the A-D converter 90 is regulated so that the signal x_o occurs at the zero crossings of the digital
65 signals following the preamble in the packet and the signal $\hat{x}$ from the equalizer 98 represents the peak of such digital signals.

The low-gain error generator **124** provides such phase regulation by operating upon successive ones of the digital signals. This may be seen from FIG. 14. In FIG. 14, two successive indications from the equalizer **98** are indicated as $\hat{x}_1$ and $\hat{x}_2$. The zero crossing between the two (2) successive indications $\hat{x}_1$ and $\hat{x}_2$ is indicated as x_o. The low gain error generator **124** in FIG. 11 adjusts the phase of the signals from the A-D converter **92** on the basis of the relative values of $\hat{x}_1$, x_o and $\hat{x}_2$ to eliminate any jitter in the phase of the digital signals from the A-D converter.

FIG. 14(a) indicates a situation where $\hat{x}_1$, x_o and $\hat{x}_2$ have no transition. Under such circumstances, no change is made in the phase of the signals produced by the A-D converter **92**, particularly since it is difficult to determine what, if any, correction should be made. FIG. 14(b) indicates a situation where $\hat{x}_1$ is positive and $\hat{x}_2$ is negative and x_o occurs before the zero crossing. Under such circumstances, the zero crossing occurs early. A phase adjustment based upon $K_3 x_o$ is made in the signals from the A-D converter **92** to delay the phase so that x_o will occur at the zero crossing. In the phase adjustment of $K_3 x_o$, K_3 is a constant gain factor. The value of K_3 is less than the value of the constant gain factor K for the situations shown in FIGS. 12(a) and 12(b) and described above.

FIGS. 14(c) and 14(d) indicate situations where x_o is late relative to the zero crossing. In FIG. 14(c), $\hat{x}_1$ is positive, x_o is negative and $\hat{x}_2$ is negative. In FIG. 14(d), $\hat{x}_1$ is negative, x_o is positive and $\hat{x}_2$ is positive. In the situations of both FIGS. 14(c) and 14(d), the A-D converter **92** delays the phase of the digital conversions produced by the A-D converter so that x_o will occur at the zero crossings. In both FIGS. 14(c) and 14(d), K_3 is the constant gain factor for advancing the phase of the digital conversions by the A-D converter **92**.

As will be seen, FIGS. 14(b), 14(c) and 14(d) indicate transitions in $\hat{x}_1$ and $\hat{x}_2$ between positive and negative values. Such transitions are accordingly designated in FIG. 14 as "Full Transitions". FIGS. 14(e), 14(f) and 14(g) indicate half transitions. In other words, $\hat{x}_1$, x_o and $\hat{x}_2$ have progressive values between a peak and a zero crossing or between a zero crossing and a peak without changing polarity. The transitions in FIGS. 14(e), 14(f) and 14(g) are accordingly designated as "Half Transitions" in FIG. 14.

In FIG. 14(e), the transition is between a positive peak for $\hat{x}_1$ and a zero value for $\hat{x}_2$. In FIG. 14(f), the transition is between a zero value for $\hat{x}_1$ and a positive peak for $\hat{x}_2$. In FIG. 14(g), the transition is between a negative peak for $\hat{x}_1$ and a zero value for $\hat{x}_2$. In each instance, the value of x_o is between the peak and the zero value.

Since only half transitions are involved in FIGS. 14(e), 14(f) and 14(g), a constant gain factor K_2 is chosen that is less than the constant gain factor K_3 for the change in the phase of the digital conversions from the A-D converter **92** as in FIGS. 14(b) and FIG. 14(c). In FIG. 14(e), the digital conversion by the A-D converter **92** is early so that the phase of the digital conversion is delayed to have x_o occur at the zero crossing. In FIG. 14(f), the digital conversion by the phase detector **92** is late so that the phase of the digital conversion is advanced to have x_o occur at the zero crossing. Similarly, the digital conversion by the phase detector **90** is delayed in FIG. 14(g) to have x_o occur at the zero crossing.

The signals from the high gain error generator **132** and the low gain error generator **124** in FIG. 11 are introduced to the loop filter **126** shown as a block in FIG. 11. The loop filter **126** operates in synchronism with the baud clock signals of twenty five megahertz (25 MHz) on the line **128**. The loop filter **126** is shown in additional detail, but on a

block diagram basis, in FIG. 15. It includes a line 170 which is schematically intended to indicate, on a generic basis, any of the line 125 (FIG. 11) from the low gain error generator 124, the line 134 from the high gain error generator 132 or
5 the line 138 from the phase inverter 136.

The signals on the line 170 in FIG. 15 are multiplied in an amplifier 172 which provides an amplification generically indicated at K_G. The amplification factor K_G for the amplifier 172 may respectively be K_3 or K_2 if the signals on the
10 line 170 are provided from the line 125 (FIG. 11) or the amplification factor may be K if the signals on the line 170 are provided from the line 134 in FIG. 11.

The signals from the amplifier 172 in FIG. 15 pass to an adder 174 which also receives signals from the output of a
15 register 176. The output from the adder 174 is introduced to the register 176. The output from the register 176 is introduced on the line 140 in FIGS. 11 and 15 to a voltage controlled oscillator (or ring oscillator) 186 in FIG. 16. The register 176 accumulates the signals from the amplifier 172
20 by the addition in the adder 174 of the signals from the amplifier and the register.

FIG. 16 shows the low gain error generator 124 and the high gain error generator 132 which are also shown in FIG. 11. The signals from the error generators 124 and 132 are
25 introduced in FIG. 16 to a select stage 180 which may constitute a multiplexer. The operation of the select stage 180 is controlled by signals on the line 146 (also shown in FIG. 11) from the controller 142 to indicate whether the signals in the packet at each instant are the timing signals in
30 the preamble or the information or data signals following the preamble. The signals from the select stage 180 in FIG. 16 pass through the loop filter 126 (also shown in FIG. 11) to a multiplexer 182, the output of which constitutes the band clock signals on the line 128 (also shown in FIG. 11).
35 The multiplexer 182 receives the signals from the voltage controlled oscillator 186 and shown within broken lines in FIG. 16. The voltage controlled oscillator includes a plurality of amplifiers in a ring relationship. Preferably sixteen (16) amplifiers are included in the ring relationship but only
40 eight (8) amplifiers 188a, 188b, 188c, 188d, 188e, 188f, 188g and 188h are shown in FIG. 16 since they provide differential outputs. The output of each amplifier in the sequence is connected to the input of the next amplifier in the sequence and the output of the last amplifier 188h in the
45 sequence in FIG. 15 is connected to the input of the first amplifier 188a in the sequence.

Each packet has signals in a unique pattern to indicate the beginning of the packet. The controller 142 (FIG. 11) senses this unique pattern of signals on the line 144 to indicate the
50 beginning of the packet. The controller 142 then produces a signal on the line 146 (FIGS. 11 and 16) to indicate whether the signals in the packet are the timing signals in the preamble or the digital signals following the preamble and representing information or data.
55 When the signal on the line 146 indicates the occurrence of the timing signals, the signals from the high gain error generator 132 in FIG. 11 and 16 pass through the select stage 180 and the loop filter 126 in FIG. 16 to the multiplexer 182. These signals activate the multiplexer 182 to pass the signals
60 from one of the amplifiers 188a–188h. By selecting on the line 140 a different one of the amplifiers 188a–188h in each cycle, the phase of the clock signals on the line 128 is adjusted in accordance with the characteristics of the signals from the high gain error generator 132. The phase-adjusted
65 clock signals are introduced to the A-D converter 92 (FIG. 7) to obtain the generation of the digital conversions by the converter.